This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (original): An apparatus for performing message passing decoding operations, the apparatus comprising:

memory including a set of memory locations for storing L sets of Z K-bit messages, where Z is a positive integer greater than one and K and L are non-zero positive integers;

a node processor including a plurality of node processing units, each node processing unit for performing at least one of a constraint node processing operation and a variable node processing operation; and

a switching device coupled the memory and to the node processing unit, the switching device for passing sets of Z K-bit messages between said memory and said node processor and for re-ordering the messages in at least one of said sets of messages in response to switch control information.

Claim 2 (original): The apparatus of claim 1, further comprising:

a message ordering control module coupled to said switching device for generating said switch control information used to control the reordering of messages in said at least one set of messages.

Claim 3 (original): The apparatus of claim 2, wherein the switching device includes circuitry for performing a message rotation operation to reorder messages included in a set of messages.

Claim 4 (original): The apparatus of claim 2, wherein the message ordering control module stores information on the order sets of messages are to be read out of the memory and information indicating what reordering of messages is to be performed by said switch on individual sets of messages read out of the memory.

Claim 5 (original): The apparatus of claim 2, wherein the message ordering control module is further coupled to said memory and sequentially generates set identifiers, each set identifier controlling the memory to access memory locations corresponding to a set of messages as part of a single read or write operation.

Claim 6 (original): The apparatus of claim 5, wherein each set identifier is a single memory address.

Claim 7 (original): The apparatus of claim 2, wherein said plurality of node processing units includes Z node processing units arranged in parallel, each one of the Z node processing units operating in parallel to process a different message in each set of Z messages passed between said memory and said node processor.

Claim 8 (original): The apparatus of claim 7, wherein said memory includes an address input which allows each set of messages to be addressed as a unit thereby enabling a set of messages to be read from said memory in a single SIMD read operation.

Claim 9 (original): The apparatus of claim 7, wherein said memory includes an address input which allows each set of messages to be addressed as a unit thereby enabling a set of messages to be written into said memory in a single SIMD write operation.

Claim 10 (original): The apparatus of claim 1, wherein each of said plurality of node processing units includes a control signal input for receiving a control signal to switch node processing unit operation between a constraint node mode of processing operation and a variable node mode of processing operation.

Claim 11 (original): The apparatus of claim 10, further comprising:

a decoder control device coupled to said plurality of node processing units, the decoder control device generating said control signal used to control said plurality of node processing units.

Claim 12 (original): The apparatus of claim 11, wherein each of the Z processing units performs a variable node low density parity check message processing operation to generate at least one new message from at least one message received from said switching device.

Claim 13 (original): The apparatus of claim 10, wherein at least one of the plurality of node processing units includes information indicating a number

of messages to be used in each of a plurality of sequential variable node processing operations.

Claim 14 (original): The apparatus of claim 7, wherein the decoder control device is further coupled to said message passing control device; and wherein the message passing control device specifies a different order in which each of the L sets of Z messages are to be read out of the memory during the variable node mode of processing operation than during constraint node mode of processing operation.

Claim 15 (original): The apparatus of claim 2, further comprising a decoder control module coupled to the message ordering module, the decoder control module including means for supplying information to the message ordering module used to control the order in which each of the L sets of Z messages are to be read out of said memory.

Claim 16 (original): The apparatus of claim 15, wherein the decoder control device further includes means for supplying an edge index to the message ordering module which controls the generation of the set identifiers supplied to said memory.

Claim 17 (original): The apparatus of claim 16, further comprising a degree memory coupled to the node processor for storing as set of node degree information.

Claim 18 (original): The apparatus of claim 17, wherein the control device further generates a node index used to determine which node degree information in the stored set of node degree information is to be supplied to the node processor at any given time.

Claims 19-49 (canceled)